Examiner Initial	Author, Title, Date, Pertinent Pages, etc.
CD	"Algebraic Survivor Memory Management Design for Viterbi Detectors", IEEE Transactions on Communications, Vol. 43, No. 9, September, 1995, 6 pages.
CD	"Generalized Trace Back Techniques for Survivor Memory Management in the Viterbi Algorithm", CH2827-4/90/0000-1318 © 1990 IEEE.
hw	"Viterbi Decoding Algorithm for Convolutional Codes with Repeat Request", IEEE Transactions on Information Theory, Vol. IT-26, No. 5, September, 1980, 8 pages.

EXAMINER	DATE CONSIDERED
[signature]	2/26/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Information Disclosure Statement PTO-1449 (Modified)

The identification of any reference is not intended to be, and should not be understood as being, an admission that such publication, in fact, constitutes "prior art" within the meaning of applicable law since, for example, a given reference may have a later effective date than first seems apparent or the reference may have an effective date which can be antedated. The "prior art" status of any reference is a matter to be resolved during prosecution.

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Sheet

Form PTO-1449 (Modified)	Atty Docket No.	Serial No.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	TI-30128	
(Use several sheets if necessary)	Applicant: Dale E. Hocevar	
	Filing Date: Herewith	Group

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date if Appropriate
	5,068,859	11/26/91	Collins et al.			
	5,327,440	07/05/94	Fredrickson et al.			
	5,469,452	11/21/95	Zehavi			
	5,781,569	07/14/98	Fossorier et al.			
	5,912,908	06/15/99	Cesari et al.			
	5,978,414	11/02/99	Nara			
	5,987,490	11/16/99	Alidina et al.			

OTHER ART

Examiner Initial	Author, Title, Date, Pertinent Pages, etc.
	"Viterbi Decoding Techniques in the TMS320C54x Family", Texas Instruments, SPRA071, June, 1996, 12 pages.
	"VLSI Structures for Viterbi Receivers: Part I - General Theory and Applications", IEEE Journal on Selected Areas in Communications, Vol. SAC-4, No. 1, January, 1986, 13 pages.
	"High-Performance VLSI Architecture for the Viterbi Algorithm", IEEE Transactions on Communications, Vol. 45, No. 2, February, 1997, 5 pages.
	"Locally Connected VLSI Architectures for the Viterbi Algorithm", IEEE Journal on Selected Areas in Communications, Vol. 6, No. 3, April, 1988, 6 pages.
	"Area-Efficient Architectures for the Viterbi Algorithm - Part 1: Theory", IEEE Transactions on Communications, Vol. 41, No. 4, April, 1993, 5 pages.
	"A Multiprocessor Architecture for Viterbi Decoders with Linear Speedup", IEEE Transactions on Signal Processing, Vol. 41, No. 9, September, 1993, 6 pages.
	"An Area-Efficient Topology for VLSI Implementation of Viterbi Decoders and Other Shuffle-Exchange Type Structures", IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, February, 1991, 4 pages.
	"An Area-Efficient Path Memory Structure for VLSI Implementation of High Speed Viterbi Decoders", Elsevier, INTEGRATION, the VLSI Journal 12 (1991) pages 79-91.